AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listing, of claims in the application:

Listing of Claims:

1. (Currently amended) A thin film transistor array panel for an X-ray detector, the thin film transistor array panel comprising:

a gate wire formed on an insulating substrate and ~~including~~ comprising a gate ~~lines~~ line and a gate electrode connected to the gate line;

a gate insulating layer formed on the gate wire;

a semiconductor layer formed on the gate insulating layer;

a data wire formed on the gate insulating layer and ~~including~~ comprising:

a data line ~~intersecting~~ which intersects the gate line~~;~~;

a source electrode connected to the data line and disposed on the semiconductor layer ~~at least in part;~~ and

a drain electrode disposed on the semiconductor layer ~~at least in part and separated~~ separate from the source electrode;

a photo diode ~~including~~ comprising:

a first electrode connected to the drain electrode;,

a second electrode ~~facing~~ which faces the first electrode~~;~~; and

a photo-conductive layer disposed between the first electrode and the second electrode;

a passivation layer disposed on the photodiode, the semiconductor layer, the data wire and the drain electrode, the passivation layer having a contact hole which exposes the second electrode;

a bias signal line disposed on the passivation layer and connected to the second electrode through the contact hole; and

a light blocking layer ~~covering~~ disposed directly on the passivation layer and the bias signal line to cover the photo diode.

2. (Currently amended) The thin film transistor array panel of claim 1, wherein the photo-conductive layer comprises a first amorphous silicon film ~~containing~~ comprising an N type impurity, a second amorphous silicon film ~~without impurity~~ disposed on the first amorphous silicon film and comprising intrinsic amorphous silicon, and a third amorphous silicon film ~~containing~~ disposed on the second amorphous silicon film and comprising a P type impurity.

3. (Currently amended) A thin film transistor array panel for an X-ray detector, the thin film transistor array panel comprising:

a gate wire formed on an insulating substrate and ~~including~~ comprising a gate ~~lines~~ line and a gate electrode connected to the gate line;

a gate insulating layer formed on the gate wire;

a semiconductor layer formed on the gate insulating layer;

a data wire formed on the gate insulating layer and ~~including~~ comprising:

a data line ~~intersecting~~ which intersects the gate line~~,~~;

a source electrode connected to the data line and disposed on the semiconductor layer ~~at least in part~~;; and

a drain electrode disposed on the semiconductor layer ~~at least in part and separated~~ separate from the source electrode;

a photo diode ~~including~~ comprising:

a first electrode connected to the drain electrode~~,~~;

a second electrode ~~facing~~ which faces the first electrode~~,~~;; and

a photo-conductive layer disposed between the first electrode and the second electrode;

a passivation layer disposed on the photodiode, the semiconductor layer, the data wire and the drain electrode, the passivation layer having a contact hole which exposes the second electrode; and

a bias signal line disposed directly on the passivation layer, connected to the second electrode through the contact hole and ~~including~~ comprising a light blocking layer ~~covering~~ which covers the photo diode.

4. (Currently amended) The thin film transistor array panel of claim 3, wherein the photo-conductive layer comprises a first amorphous silicon film ~~containing~~ comprising an N type impurity, a second amorphous silicon film ~~without impurity~~ disposed on the first amorphous silicon film and comprising intrinsic

amorphous silicon, and a third amorphous silicon film ~~containing~~ disposed on the second amorphous silicon film and comprising a P type impurity.

5. (Currently amended) A thin film transistor array panel for an X-ray detector, the thin film transistor array panel comprising:

a gate wire formed on an insulating substrate and ~~including~~ comprising a gate ~~lines~~ line and a gate electrode connected to the gate line;

a gate insulating layer formed on the gate wire;

a semiconductor layer formed on the gate insulating layer;

a data wire formed on the gate insulating layer and ~~including~~ comprising:

a data line ~~intersecting~~ which intersects the gate line~~,~~;

a source electrode connected to the data line and disposed on the semiconductor layer ~~at least in part~~,; and

a drain electrode disposed on the semiconductor layer ~~at least in part and separated~~ separate from the source electrode;

a photo diode ~~including~~ comprising:

a first electrode connected to the drain electrode~~,~~;

a second electrode ~~facing~~ which faces the first electrode~~,~~; and

a photo-conductive layer disposed between the first electrode and the second electrode; and

a bias signal line connected to the second electrode,

wherein

the semiconductor layer is disconnected in a region disposed between the source electrode and the drain electrode, and

the region disposed between the source electrode and the drain electrode is absent semiconductor material to transmit a signal to the data line.

6. (Currently amended) The thin film transistor array panel of claim 5, wherein the photo-conductive layer comprises a first amorphous silicon film ~~containing~~ comprising an N type impurity, a second amorphous silicon film ~~without impurity~~ disposed on the first amorphous silicon film and comprising intrinsic amorphous silicon, and a third amorphous silicon film disposed on the second amorphous silicon film and ~~containing~~ comprising a P type impurity.